

Amendment and Response

Applicant: Michael Goessel et al.

Serial No.: 10/577,288

Filed: April 24, 2006

Docket No.: I431.135.101/FIN516PCT/US

Title: EVALUATION CIRCUIT AND METHOD FOR DETECTING AND/OR LOCATING FAULTY DATA WORDS IN A DATA STREAM T_N

REMARKS

The following remarks are made in response to the Non-Final Office Action mailed June 10, 2009. Claim 53 has been allowed. Claims 35-52 and 55-58 were rejected. With this Response, claim 35 has been amended. Claims 35-53 and 55-58 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 103

Claims 35-37, 39, 41-45, 48-52, and 55 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Hasegawa et al. U.S. Publication 2004/0246337 (“Hasegawa”), in view of Meaney, U.S. Patent 6, 055,660 (“Meaney”). Claims 38, 40, 46, 47 and 56-58 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Hasegawa and Meaney in view of additional references. Applicants respectfully traverse these rejections.

Claim 35 has been amended to more clearly recite the claimed subject matter. As such, claim 35 includes “the first linear automaton circuit and the second linear automaton circuit each have inputs that are commonly connected for receiving a data stream T_n comprising n successive data words.” Further, claim 35 has been amended to note that the state vectors are represented by the character z .

In the response to arguments section, the Office Action states, “compression is a well known technique,” and that non-serial data word signatures are not recited in the rejected claims. Office Action at p. 3. However, to establish *prima facie* obviousness, all claim limitations must be considered. MPEP 2143.03 (citing *In re Wilson*, 424 F.2d 1382, 1385, (CCPA 1970)). Further, the claimed invention as a whole must be considered, and distilling the claimed device down to the “gist” or “thrust” of an invention disregards the requirement of analyzing the subject matter “as a whole.” MPEP 2141.02 (citing *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983)).

Applicants respectfully submit that in generally referring to “compression,” the Office Action is distilling the claimed subject matter to the “gist” of the invention. Further, Applicants

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respectfully submit that non-serial word signatures are recited in claim 35, and this claim element must be considered.

Claim 35 includes $z(t+1) = Az(t) \oplus y(t)$. This equation shows that not only one element of the data word y is compressed, but the complete data word y having a width of k bits is compressed. Otherwise, A would not be a matrix.

As such, Hasagawa fails to teach a first signature and a second signature, respectively, can be calculated of each data word.

Applicants further respectfully contend that combining the disclosure of Hasegawa with Meaney as proposed in the Office Action would change the principle of operation of the Hasegawa reference, because the MISR B provides a compression of a data word. Implementing MISR B in the scan compression unit 2 of Hasegawa would lead to completely different circuit and a completely different function than Hasegawa provides.

Further, the MISR B cannot be described by the equation $z(t+1) = Bz(t) \text{ XOR } y(t)$, because the MISR B does not have the data word $y(t)$ as input. The MISR A and MISR B are not connected in parallel. However, the MISR A is provided to compress the output of a first chip, the output being received via the bus A, whereas the MISR B is used to check the output data of a second chip, the output data being provided via the bus B.

Thus, Meaney discloses comparing outputs of two different chips – comparing two separate data words. This is different than examining a sequence of a single data word.

In response, the Office Action states on page 4 that MISR A and MISR B (disclosed in Meaney) will receive the same data as results. However, Meaney teaches on page 2, lines 56 to 58 that the goal is to compare the control and/or data signals with Bus A and Bus B, 11 and 11', to determine if the two chips get out of synchronization. Thus, the disclosed circuit functions to detect whether the buses 11 and 11' *differ*. Accordingly, the data words at buses 11 and 11' are not connected to the same input line. If the buses 11 and 11' were connected together, they could not differ and get out of synchronization. The purpose of the circuit is to detect differences between the two data words. It follows from this that the data words input must differ.

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Applicants therefore believe the Office Action fails to establish *prima facie* obviousness. Claim 35, and the claims dependent thereon, are thus allowable over Hasegawa and Meaney.

Allowable Subject Matter

The Office Action noted that claim 53 was allowed. The Examiner's acknowledgement of the allowed claim is appreciated.

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CONCLUSION

In view of the above, Applicant respectfully submits that all of the pending claims are in form for allowance. Therefore, reconsideration and withdrawal of the rejections and allowance of the claims are respectfully requested.

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Mark L. Gleason at Telephone No. (612) 767-2503, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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